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| EXAMINER |
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| TSAI, TSUNG YIN |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| | Application No. | Applicant(s) |
| :--- | :--- | :--- |
| **Office Action Summary** | 10/759,583 | KLOTH, AXEL K. |
| | **Examiner** | **Art Unit** | |
| | Tsung-Yin Tsai | 2624 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>26 June 2007</u>.

2a)☒ This action is **FINAL.** 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) <u>1-17</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-17</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>14 June 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAIL ACTION

Acknowledge of amendment received on 7/3/2007 and made of record.

Acknowledge of amendment to specification.

Acknowledge of amendment to claims 1 and 9 and the supports for the amended

limitation of the claims from the specification.

Acknowledge of addition of claims 16 and 17.

Acknowledge of figure 7 with no changes.

### *Response to Arguments*

**Applicant's argument** – Amended of specification for paragraph 0033 and 0037 as

requested by the Examiner.

**Examiner's response** – Withdraw of objection of the specification due to amended

correction.

**Applicant's argument** – Withdraw of objection of figure 7.

**Examiner's response** – Applicant called and clarify objection regarding figure 7. No

change are request on the figure 7 anymore, thus, objection to figure 7 is withdrawn.

**Applicant's argument** – Claims 1-15 stand rejected under 35 U.S.C. 103(a) as being

unpatentable over Juvinall (US Patent No. 5,214,713), hereinafter referred to as

Juvinall, in view of Chen et al. (U.S. Patent No. 5,535,288), hereinafter referred to as

Chen. Applicant respectfully traverses these rejections due to the following reasons:

- Juvinall processes two lines of data at a time and not one frame at a time

- Juvinall fails to teach or suggest claim 1 which recites, in part, " an image

  processing engine adapted to perform object-independent processing

  corresponding to a first layer of the image processing system to ~generate

  a first set of processed data, said image processing engine further

  adapted to include a plurality of processors each associated with a

  different one of pixels of the image frame; and a post processing engine

  adapted to directly receive the first set of processed data and to perform

  object-dependent processing corresponding to a second processing layer

  of the image processing system on the received first set of processed data

  thereby to generate a second set of processed data, said post processing

  engine further adapted to include an N-way symmetric multi-processing

  system (SMP) having disposed therein N DFT engines and N matrix

  multiplication engines; wherein N is an integer greater than 1."

- Chen also fails to teach or suggest "a post processing engine adapted to

  directly receive the first set of processed data and to perform object-

  dependent processing corresponding to a second processing layer of the

  image processing system on the received first set of processed data

  thereby to generate a second set of processed data, said post processing

  engine further adapted to include an N-way symmetric multi-processing

system (SMP) having disposed therein N DFT engines and N matrix

multiplication engines; wherein N is an integer greater than 1"

- Claim 9 and its dependent claims 10-16 are allowable over Juvinall in view

  of Chen for at least the same reasons as is claim 1.

**Examiner's response** – The combination of Juvinall and Chen teaches that following:

- Juvinall processes the image frame (Further on column 10 lines 3-25 and

  with addition of figure 9 discloses that it is not necessarily to process the

  whole image as a whole, but the image is process neverless. Applicant is

  concern regarding processing operation to be improve by pipeline to

  improve efficiceny and viewing the object. Reduction of the data, as taught

  by Juvinall, to be process will not overload the pipeline and this will

  improve efficiency of memory storage space and lower require processing

  power. Reduction of the image mean that the view of field is strictly of the

  object only and not any of the background data. Figure 9 discloses how

  the data is selectively removed from the whole image, thus, leaving only

  the object in view only before processing. )

- Juvinall combine with Chen teaches " an image processing engine

  (Juvinall. Figure 1 disclose a whole system that does image processing,

  column 2 lines 10-40 disclose image processing computers) adapted to

  perform object-independent processing (Juvinall. figure 2 discloses that

  the object of interest for processing is that of the bottle-cap, where is seen

  independent of the bottle for processing) corresponding to a first layer of

the image processing system (Juvinall. figure 1 is seen as the first lay of

the image processing system, which is the hardware to obtain the image

data) to generate a first set of processed data (Juvinall. figure 2 disclose

bottle-cap for image processing, this is first set of data that is obtain from

the first layer image processing system for processing), said image

processing engine (Juvinall. Figure 1 disclose a whole system that does

image processing, column 2 lines 10-40 disclose image processing

computers) further adapted to include a plurality of processors each

associated with a different one of pixels of the image frame (Juvinall.

column 2 lines 50-55 further disclose a plurality of one-bit data processor

configure in an array, column 2 lines 60-67 disclose where each of the

processor receives and operates on one pixel data at a time, thus this is

seen as processing a different pixel of the image); and a post processing

engine (Juvinall. column 2 lines 50-55 further disclose a plurality of one-bit

data processor configure in an array, this is the post processing engine)

adapted to directly receive the first set of processed data (Juvinall. column

2 lines 50-55 further disclose a plurality of one-bit data processor

configure in an array, where we can see that this array of processor than

process the first set of data that is given to them by the master computer

that control the control data buses) and to perform object-dependent

processing (Juvinall. figure 2 discloses that the object of interest for

processing is that of the bottle-cap, where is seen independent of the

bottle for processing) corresponding to a second processing layer

(Juvinall. Figure 6 is second processing layer, which are the array of one-

bit processors) of the image processing system on the received first set of

processed data thereby to generate a second set of processed data

(Juvinall. column 2 lines 65-68 discloses where the data is process by the

array of processor and return the process data to memory, column 4 lines

55-65 discloses where the data is use for image comparison), said post

processing engine (Juvinall. column 2 lines 50-55 further disclose a

plurality of one-bit data processor configure in an array, this is the post

processing engine) further adapted to include an N-way symmetric multi-

processing system (SMP) (Chen teaches Juvinall. figure 6 discloses a

symmetric processing system, where the symmetry is of N=2, therefore

symmetric) having disposed therein N DFT engines (Chen teaches

Juvinall. Figure 6 step 2 discloses the symmetric DFT engines) and N

matrix multiplication engines (Chen teaches Juvinall. Figure 6 discloses

the matrix of multiplication of engines, where the engines are of combining

engines, DFT rows, DFT columns, split and multiplying engines in the

whole system); wherein N is an integer greater than 1."

- Regarding where Chen also fails to teach or suggest "a post processing

    engine adapted to directly receive the first set of processed data and to

    perform object-dependent processing corresponding to a second

    processing layer of the image processing system on the received first set

of processed data thereby to generate a second set of processed data,

said post processing engine further adapted to include an N-way

symmetric multi-processing system (SMP) having disposed therein N DFT

engines and N matrix multiplication engines; wherein N is an integer

greater than 1". Juvinall teaches regarding the part of the limitation from "a

post processing engine adapted to directly receive the first set of

processed data and to perform object-dependent processing

corresponding to a second processing layer of the image processing

system on the received first set of processed data thereby to generate a

second set of processed data, said post processing engine" as stated

above. And Chen further teaches Juvinall regarding "an N-way symmetric

multi-processing system (SMP) having disposed therein N DFT engines

and N matrix multiplication engines; wherein N is an integer greater than

1." It is the combination of Juvinall and Chen that teaches all the limitation

of claim 1. The motivation to combine Juvinall and Chen is that Chen help

further clarify the design of this kind of processing system with a draw

diagram already. Chen further states that this design of processing will

provide the optimal use of computation (Chen. Column 7 lines 15-20) as

well as performing two simultaneous 2D cross correlations of data sets

(Chen. Column 8 lines 7-10).

- Claim 9 and its dependent claims 10-16 are rejected over Juvinall in view

  of Chen for the same reasons as is claim 1 as stated above.

## *Claim Rejections – 35 USC 103*

1.      The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.      Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Juvinall (US Patent Number 5,214,713. IDS) in view of Chen et al (US Patent Number

5,535,288).

(1) Regarding claim 1:

Juvinall teaches the following subject matter:

an image processing engine ( Figure 1 disclose a whole system that does

image processing, column 2 lines 10-40 disclose image processing computers)

adapted to perform object-independent processing (figure 2 discloses that the

object of interest for processing is that of the bottle-cap, where is seen

independent of the bottle for processing) corresponding to a first layer of the

image processing system (figure 1 is seen as the first lay of the image

processing system, which is the hardware to obtain the image data) to generate

a first set of processed data (figure 2 disclose bottle-cap for image processing,

this is first set of data that is obtain from the first layer image processing system

for processing), said image processing engine ( Figure 1 disclose a whole

system that does image processing, column 2 lines 10-40 disclose image

processing computers) further adapted to include a plurality of processors each

associated with a different one of pixels of the image frame ( column 2 lines 50-

55 further disclose a plurality of one-bit data processor configure in an array,

column 2 lines 60-67 disclose where each of the processor receives and

operates on one pixel data at a time, thus this is seen as processing a different

pixel of the image); and a post processing engine ( column 2 lines 50-55 further

disclose a plurality of one-bit data processor configure in an array, this is the post

processing engine) adapted to directly receive the first set of processed data (

column 2 lines 50-55 further disclose a plurality of one-bit data processor

configure in an array, where we can see that this array of processor than process

the first set of data that is given to them by the master computer that control the

control data buses) and to perform object-dependent processing ( figure 2

discloses that the object of interest for processing is that of the bottle-cap, where

is seen independent of the bottle for processing) corresponding to a second

processing layer ( Figure 6 is second processing layer, which are the array of

one-bit processors) of the image processing system on the received first set of

processed data thereby to generate a second set of processed data (column 2

lines 65-68 discloses where the data is process by the array of processor and

return the process data to memory, column 4 lines 55-65 discloses where the

data is use for image comparison), said post processing engine ( column 2 lines

50-55 further disclose a plurality of one-bit data processor configure in an array,

this is the post processing engine)

Juvinall does not disclose the said post processing engine further adapted to include an N-way symmetric multi-processing system (SMP) having disposed therein N DFT engines and N matrix multiplication engines; wherein N is an integer greater than 1; post-processing engine in detail, wherein, Chen et al further provide the details for the post-processing engine.

However, Chen et al disclose include an N-way symmetric multi-processing system (SMP) (figure 6 discloses a symmetric processing system, where the symmetry is of N=2, therefore symmetric) having disposed therein N DFT engines (Figure 6 step 2 discloses the symmetric DFT engines) and N matrix multiplication engines (Figure 6 discloses the matrix of multiplication of engines, where the engines are of combining engines, DFT rows, DFT columns, split and multiplying engines in the whole system); wherein N is an integer greater than 1."

It would have been obvious to one skill in the art at the time of the invention to employ Chen et al teachings to Juvinall to clarify the design of the post-processing engine. In doing so, the design structure of this post-processing engine provides the optimal use of computation (column 7 lines 15-20) as well as performing two simultaneous 2-dimensional cross correlations of data sets (column 8 lines 7-10).

(2) Regarding claim 2:

Juvinall further disclose the plurality of processors of the image processing

engine form a massively parallel processing system (94-96 figure 5, column 7

lines 53-67 to column 8 lines 1-24. The parallel processing system is describe.).

(3) Regarding claim 3:

Juvinall further disclose the massively parallel processing system is a

systolic array type massively parallel processing system (84-86 figure 4, 94-96

figure 5, column 2 lines 55-60. Where the system is in a systolic array matrix type

format.).

(4) Regarding claim 4:

Juvinall further disclose the systolic array type massively parallel

processing system is configured as a single-instruction multiple-data system

(column 2 lines 60-67, column 3 lines 45-63. Single-instruction system is

describe.).

(5) Regarding claim 5:

Juvinall further disclose each of the plurality of the processors is further

adapted to perform a unified and symmetric processing of N dimensions in space

and one dimension in time (column 9 lines 3-45, column 9 lines 24-30. A

dimension for the image format is described as being process one after another,

suggesting the passage of time.).

(6) Regarding claim 6:

Juvinall further disclose an image capturing block (48 figure 1, 48 figure 3, 76 figure 4, column 1 lines 29-33, column 2 lines 46-49, column 1 lines 66-67, column 10 lines 3-24. A camera and/or CCD are presented in the invention.).

(7) Regarding claim 7:

Juvinall further disclose the plurality of processors are formed on a first semiconductor substrate different from a second semiconductor substrate on which the image capturing block is formed (column 6 lines 64-67 to column 7 lines 1-17. CCD and/or camera is couple to the interface that has the plurality of processor, thus they are all on different substrates.).

(8) Regarding claim 8:

Juvinall further disclose a realignment buffer adapted to realign the data received from first and second analog-to-digital converters disposed in the image capturing block (column 8 lines 48-67 to column 9 lines 1-21. When the systolic array of processors request data, the main processor will alignment the buffer with data using FIFO method to feed the data to the processor matrix.).

(9) Regarding claim 9:

Juvinall teaches the following subject matter:

performing object-independent processing (figure 2 discloses that the object of interest for processing is that of the bottle-cap, where is seen independent of the bottle for processing) corresponding to a first image processing layer (figure 1 is seen as the first lay of the image processing system, which is the hardware to obtain the image data) to generate a first set of

processed data (figure 2 disclose bottle-cap for image processing, this is first set

of data that is obtain from the first layer image processing system for

processing);

supplying the first set of processed data (figure 2 disclose bottle-cap for

image processing, this is first set of data that is obtain from the first layer image

processing system for processing) directly to a second processing layer (Figure 6

is second processing layer, which are the array of one-bit processors);

performing object-dependent processing (figure 2 discloses that the object of

interest for processing is that of the bottle-cap, where is seen independent of the

bottle for processing) corresponding to the second processing layer (Figure 6 is

second processing layer, which are the array of one-bit processors) on the

received first set of processed data (figure 2 disclose bottle-cap for image

processing, this is first set of data that is obtain from the first layer image

processing system for processing) thereby to generate a second set of

processed data (column 2 lines 65-68 discloses where the data is process by the

array of processor and return the process data to memory, column 4 lines 55-65

discloses where the data is use for image comparison).

Juvinall does not disclose the post processing engine further adapted to

include an N-way symmetric multi-processing system (SMP) having disposed

therein N DFT engines and N matrix multiplication engines; wherein N is an

integer greater than 1.

However, Chen et al disclose include an N-way symmetric multi-processing system (SMP) (figure 6 discloses a symmetric processing system, where the symmetry is of N=2, therefore symmetric) having disposed therein N DFT engines (Figure 6 step 2 discloses the symmetric DFT engines) and N matrix multiplication engines (Figure 6 discloses the matrix of multiplication of engines, where the engines are of combining engines, DFT rows, DFT columns, split and multiplying engines in the whole system); wherein N is an integer greater than 1."

It would have been obvious to one skill in the art at the time of the invention to employ Chen et al teachings to Juvinall to clarify the design of the post-processing engine. In doing so, the design structure of this post-processing engine provides the optimal use of computation (column 7 lines 15-20) as well as performing two simultaneous 2-dimensional cross correlations of data sets (column 8 lines 7-10).

(10) Regarding claim 10:

Juvinall further disclose performing object independent processing by a plurality of processors that form a massively parallel processing system (94-96 figure 5, column 7 lines 53-67 to column 8 lines 1-24. The parallel processing system is describe.).

(11) Regarding claim 11:

Juvinall further disclose the massively parallel processing system is a systolic array type massively parallel processing system (84-86 figure 4, 94-96

figure 5, column 2 lines 55-60. Where the system is in a systolic array matrix type

format).

(12) Regarding claim 12:

   Juvinall further disclose configuring the systolic array massively parallel

processing system as a single-instruction multiple-data system (column 2 lines

60-67, column 3 lines 45-63. Single-instruction system is describe.).

(13) Regarding claim 13:

   Juvinall further disclose each of the plurality of the processors is further

adapted to perform a unified and symmetric processing of N dimensions in space

and one dimension in time (column 9 lines 3-45, column 9 lines 24-30. A

dimension for the image format is described as being process one after another,

suggesting the passage of time.).

(14) Regarding claim 14:

   Juvinall further disclose capturing the image frame on a first

semiconductor substrate that is different from a second semiconductor substrate

on which the plurality of processors are formed (column 6 lines 64-67 to column

7 lines 1-17. CCD and/or camera is couple to the interface that has the plurality

of processor, thus they are all on different substrates).

(15) Regarding claim 15:

   Juvinall further disclose converting analog data corresponding to the

image frame to digital data; and realigning the converted digital data (column 8

lines 48-67 to column 9 lines 1-21. When the systolic array of processors request

data, the main processor will alignment the buffer with data using FIFO method

to feed the data to the processor matrix. The inherit function of the CCD is to

convert analog single to that of digital data in order for the processors to process

it.).

(16) Regarding claims 16 and 17:

Juvinall further teaches performing object composition (figure 2 disclose a

bottle-cap itself, this is seen as the objection composition in the field of view),

recognition (column 10 lines 3-25 disclose where the image data is selected from

memory to be processing, where the reason for selected data is to separate the

data that is only concern the object that is recognize for processing) and

association corresponding to a third processing layer (column 4 lines 55-65

disclose where the process data is than compare, the comparing process is seen

as the third processing layer).

## *Conclusion*

3.      Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

4.     The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

Pechanek et al (US Patent Number 6,405,185 B1) disclose massively parallel

array processor.

Wilkinson et al (US Patent Number 5,713,037) disclose slide bus communication

functions for SIMD/MIMD array processor.

Coldren et al (US Patent Number 4,707,647) disclose gray scale vision method
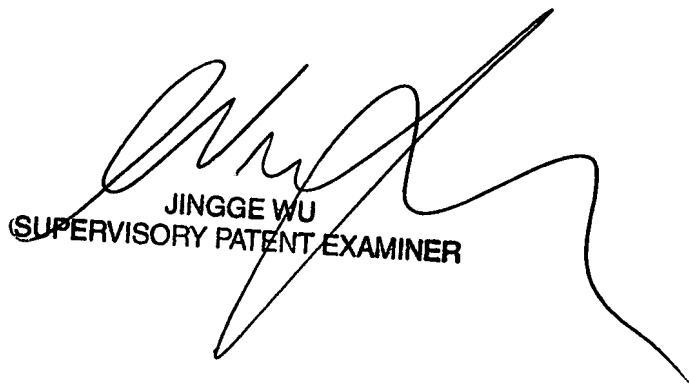
and system utilizing same.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tsung-Yin Tsai whose telephone number is (571) 270-

1671. The examiner can normally be reached on Monday - Friday  8 am - 5 pm ESP.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Jingge Wu can be reached on (571)272-7429. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tsung-Yin Tsai
July 12, 2007

JINGGE WU
(SUPERVISORY PATENT EXAMINER